AMENDMENTS TO THE CLAIMS

Claims 1-20 (cancelled)

Claim 21 (currently amended): A system for critical parameter analysis (CPA) of a semiconductor device (DUT), comprising:

a laser scanning microscope (LSM);

automated test apparatus (ATE) for providing predefined stimulus to the semiconductor device (DUT), for comparing responses from the semiconductor device (DUT) against a set of predefined expected responses, and for generating a short output pulse when a difference is detected between responses from said semiconductor device (DUT) and said predefined expected responses~~;~~, said automated test apparatus being connected to the DUT while the DUT is disposed ~~means for disposing said semiconductor device (DUT)~~ within a scanning chamber of said laser scanning microscope (LSM) ~~while said semiconductor device (DUT) is connected to said automated test apparatus (ATE)~~;

display means for displaying an image of said semiconductor device produced by said laser scanning microscope (LSM);

means for overlaying a visible representation of said short output pulse on said displayed image to indicate a corresponding position on the semiconductor device (DUT) of a scanning beam of the laser scanning microscope (LSM) at the time the output pulse was generated; and

means for ~~repeatedly applying said predefined stimulus to said semiconductor device (DUT) and comparing responses therefrom against said predefined expected responses while~~ simultaneously scanning said semiconductor device (DUT) with said laser scanning microscope (LSM) while said ATE repeatedly applies said predefined stimulus to said DUT and compares responses therefrom against said predefined expected responses;

wherein

the automated test apparatus (ATE) and the semiconductor device (DUT) form a closed loop feedback system;

~~wherein~~ the automated test apparatus (ATE) is programmed to 'break' in or out of a vector loop which is detecting pass/fail operation of the semiconductor device (DUT); and

~~wherein~~ said automated test apparatus (ATE) is configured to repeatedly cycle ("short-cycle") said predefined stimulus from a starting point up to a point of failure when such failure is detected.

Claim 22 (previously presented): A system according to claim 21, wherein said semiconductor device (DUT) is fixtured such that ATE connections to the device are made within a scanning chamber of the laser scanning microscope (LSM).

Claim 23 (currently amended): A system according to claim 21, further comprising:

image converting means for representing output from ~~said~~ the laser scanning microscope (LSM) as a viewable video signal and for overlaying the output signal indication from the automated test apparatus (ATE) on said viewable video signal; and

display means for viewing said video signal with overlaid automated test apparatus (ATE) output signal indication.

Claim 24 (currently amended): A system according to claim 23, wherein said overlaid ATE output signal indication produces a visible spot on said display means at a location on a simultaneously displayed image of the semiconductor device (DUT) that indicates the location on the semiconductor device (DUT) that was illuminated by ~~the~~ the laser scanning microscope (LSM) at the time the automated test apparatus (ATE) output signal indication was produced.

Claim 25 (previously presented): A system according to claim 21, wherein said predefined stimulus is provided to said automated test apparatus (ATE) in the form of a set of test vectors.

Claim 26 (previously presented): A system according to claim 21, wherein said predefined expected responses are provided to said automated test apparatus (ATE) in the form of a set of test vectors.

Claim 27 (previously presented): A system according to claim 21, wherein said automated test apparatus (ATE) is configured to repeatedly apply said predefined stimulus to said semiconductor device (DUT) in a test "loop."

Claim 28 (previously presented): A system according to claim 21, wherein said output pulse is a short pulse generated when a difference is detected between responses by said semiconductor device (DUT) to said predefined stimulus and the predefined expected responses.

Claim 29 (currently amended): A method for critical parameter analysis (CPA) of a semiconductor device (DUT), comprising:

providing a focused optical beam scanning device;

providing automated test apparatus (ATE) for providing predefined stimulus to the semiconductor device (DUT), for comparing responses from the semiconductor device (DUT) against a set of predefined expected responses, and for generating a short output pulse when a difference is detected between responses from said semiconductor device (DUT) and said predefined expected responses~~;~~ , said automated test apparatus being connected to the DUT while the DUT is disposed ~~means for disposing said semiconductor device (DUT)~~ within a scanning chamber of said laser scanning microscope (LSM) ~~while said semiconductor device (DUT) is connected to said automated test apparatus (ATE)~~;

~~display means for~~ displaying an image of said semiconductor device produced by said laser scanning microscope (LSM);

~~means for~~ overlaying a visible representation of said short output pulse on said displayed image to indicate a corresponding position on the semiconductor device (DUT) of a scanning beam of the laser scanning microscope (LSM) at the time the output pulse was generated; and

~~means for repeatedly applying said predefined stimulus to said semiconductor device (DUT) and comparing responses therefrom against said predefined expected responses while~~ simultaneously scanning said semiconductor device (DUT) with said laser scanning microscope

(LSM) while repeatedly applying said predefined stimulus to said DUT and comparing responses therefrom against said predefined expected responses using said ATE;

wherein

the automated test apparatus (ATE) and the semiconductor device (DUT) form a closed loop feedback system;

~~wherein~~ the automated test apparatus (ATE) is programmed to 'break' in or out of a vector loop which is detecting pass/fail operation of the semiconductor device (DUT); and

~~wherein~~ said automated test apparatus (ATE) is configured to repeatedly cycle ("short-cycle") said predefined stimulus from a starting point up to a point of failure when such failure is detected.

Claim 30 (previously presented): A method according to claim 29, wherein said focused optical beam scanning device is a laser scanning microscope (LSM).

Claim 31 (previously presented): A method according to claim 29, wherein the automated test apparatus (ATE) is synchronized with the focused optical beam scanning device.

Claim 32 (previously presented): A method according to claim 29, further comprising providing optical signatures that only appear on the gate level devices responsible for the failing test.

Claim 33 (previously presented): A method according to claim 29, further comprising providing real time feedback to the focused optical beam scanning device and subsequent optical images acquired.

Claim 34 (previously presented): A method according to claim 29, further comprising:

fixturing said semiconductor device (DUT) such that ATE connections to the device are made within a scanning chamber of the focused optical beam scanning device.

Claim 35 (currently amended): A method according to claim 29, further comprising:

representing an output from ~~said~~ the focused optical beam scanning device as a viewable video signal and for overlaying the output signal indication from the automated test apparatus (ATE) on said viewable video signal; and

~~display means for~~ viewing said video signal with overlaid automated test apparatus (ATE) output signal indication.

Claim 36 (currently amended): A method according to claim 35, wherein said overlaid ATE output signal indication produces a visible spot on said display means at a location on a simultaneously displayed image of the semiconductor device (DUT) that indicates the location on the semiconductor device (DUT) that was illuminated by ~~the~~ the focused optical beam scanning device at the time the automated test apparatus (ATE) output signal indication was produced.

Claim 37 (previously presented): A method according to claim 29, wherein said predefined stimulus is provided to said automated test apparatus (ATE) in the form of a set of test vectors.

Claim 38 (previously presented): A method according to claim 29, wherein said predefined expected responses are provided to said automated test apparatus (ATE) in the form of a set of test vectors.

Claim 39 (previously presented): A method according to claim 29, wherein said automated test apparatus (ATE) is configured to repeatedly apply said predefined stimulus to said semiconductor device (DUT) in a test "loop."

Claim 40 (previously presented): A method according to claim 29, wherein said output pulse is a short pulse generated when a difference is detected between responses by said semiconductor device (DUT) to said predefined stimulus and the predefined expected responses.